FIG. 1

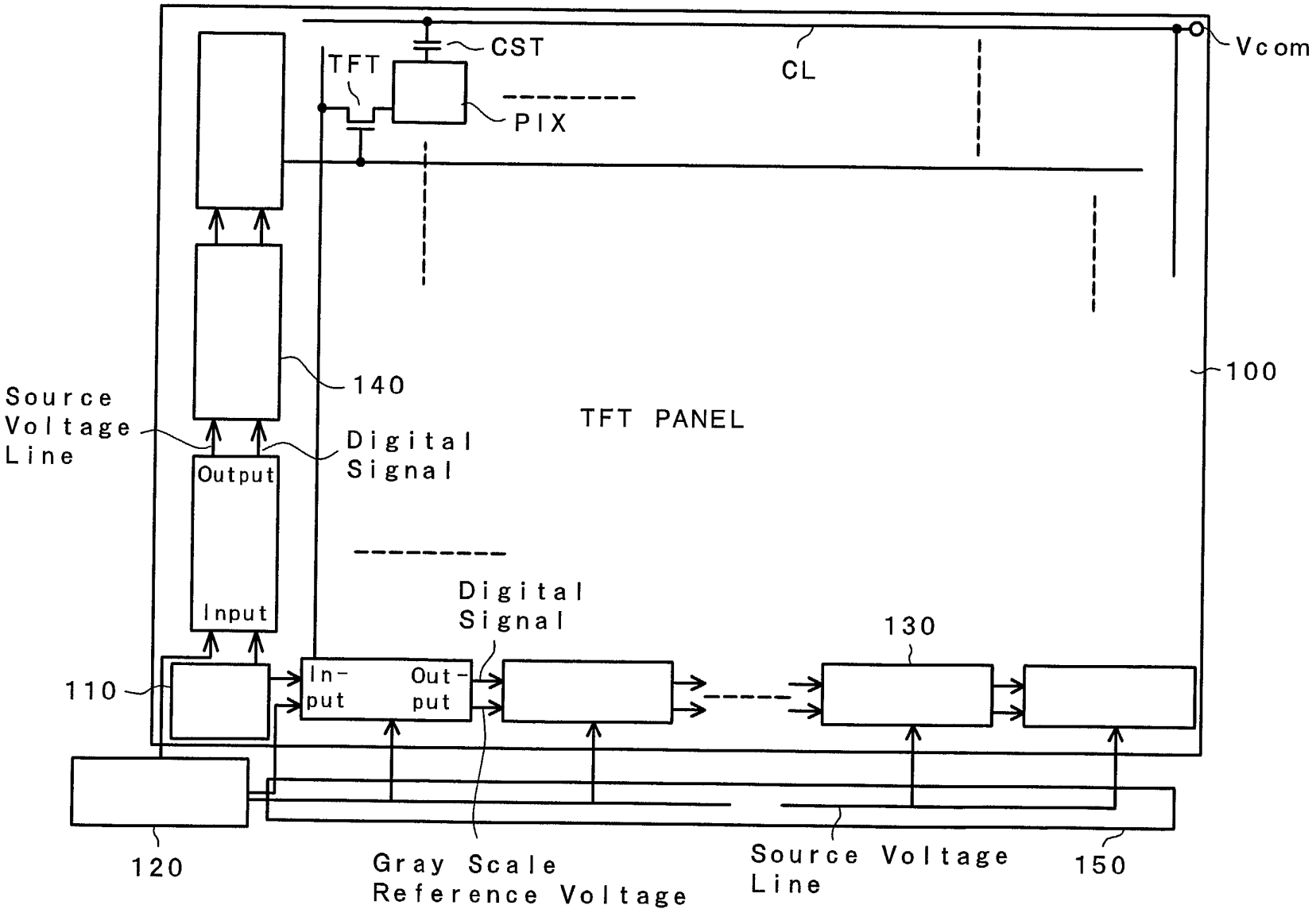
CST
TFT
PIX
CL
Vcom
100
140
Source
Voltage
Line
Digital
Signal
Output
Input
TFT PANEL
Digital
Signal
130
110
In-
put
Out-
put
120
Gray Scale
Reference Voltage
Source Voltage
Line
150

FIG. 2

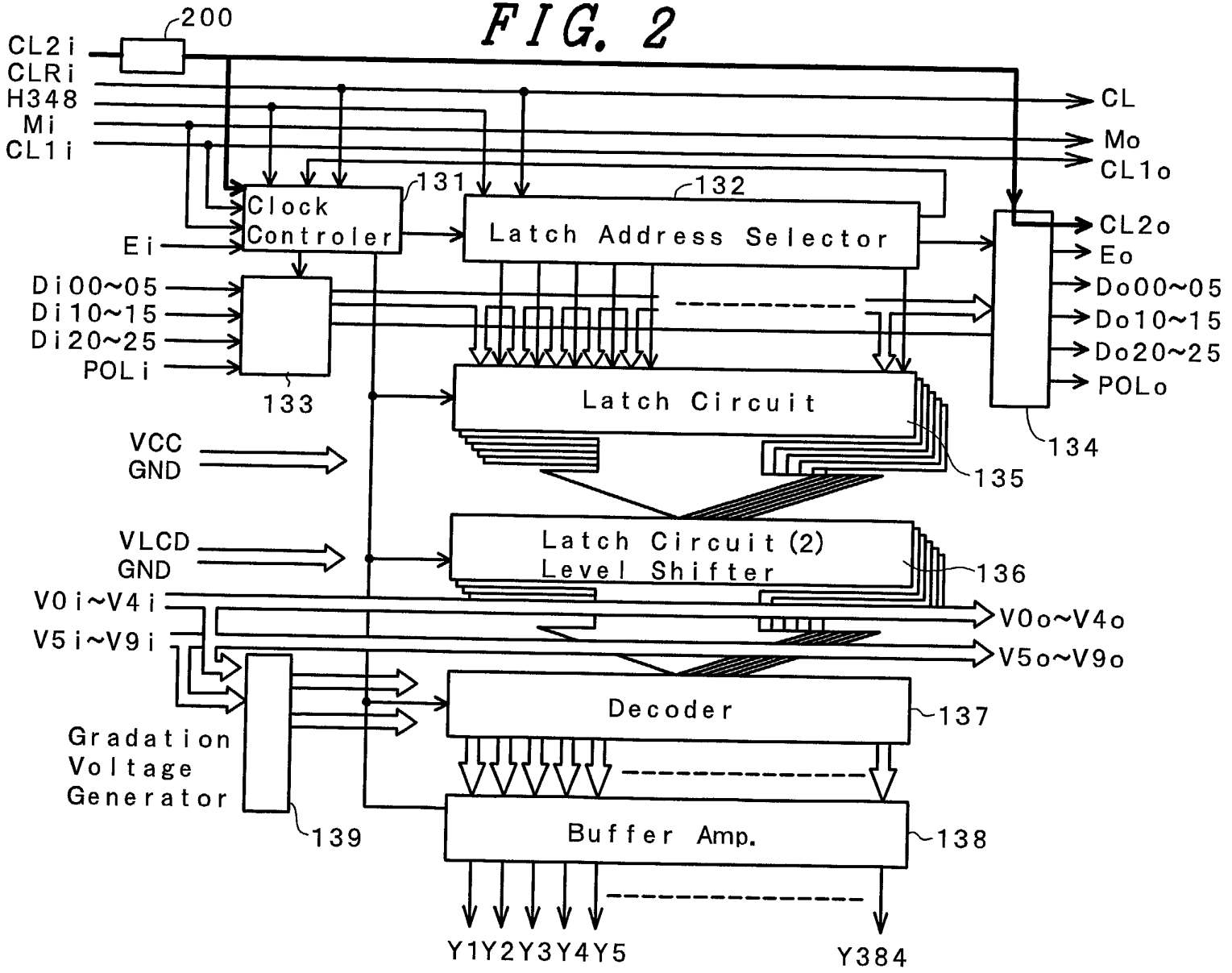
200
CL2i
CLRi
H348
Mi
CL1i
CL
Mo
CL1o
131
132
Clock Controler
Latch Address Selector
Ei
CL2o
Eo
Do00~05
Do10~15
Do20~25
POLo
Di00~05
Di10~15
Di20~25
POLi
133
Latch Circuit
134
135
VCC
GND
VLCD
GND
Latch Circuit (2)
Level Shifter
136
V0i~V4i
V5i~V9i
V0o~V4o
V5o~V9o
Decoder
137
Gradation
Voltage
Generator
139
Buffer Amp.
138
Y1Y2Y3Y4Y5
Y384

FIG. 3

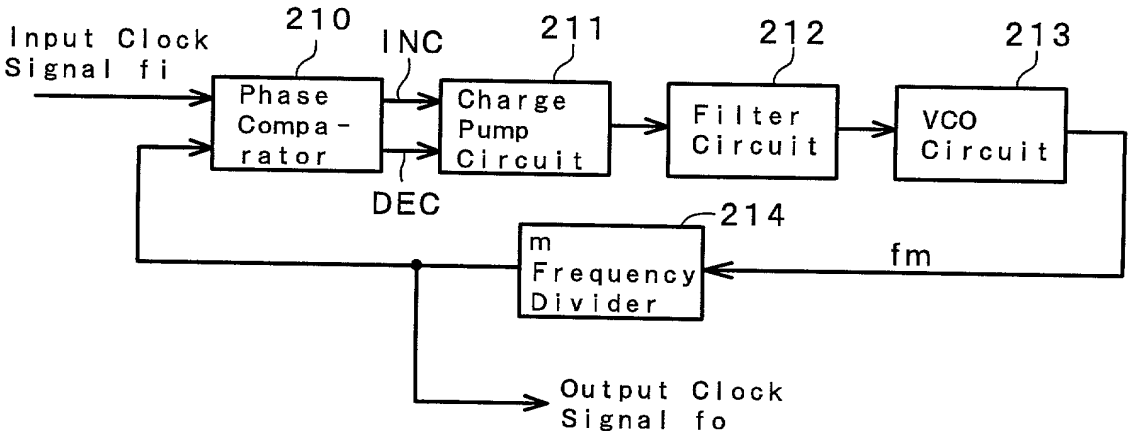

FIG. 4

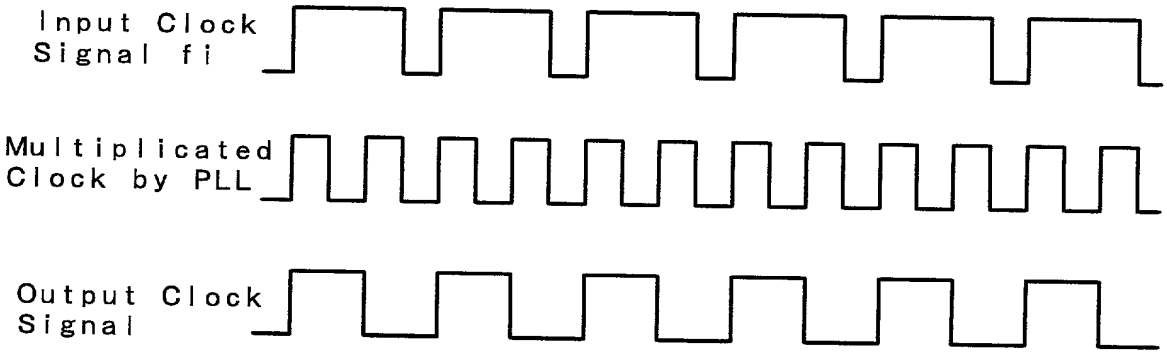

FIG. 5

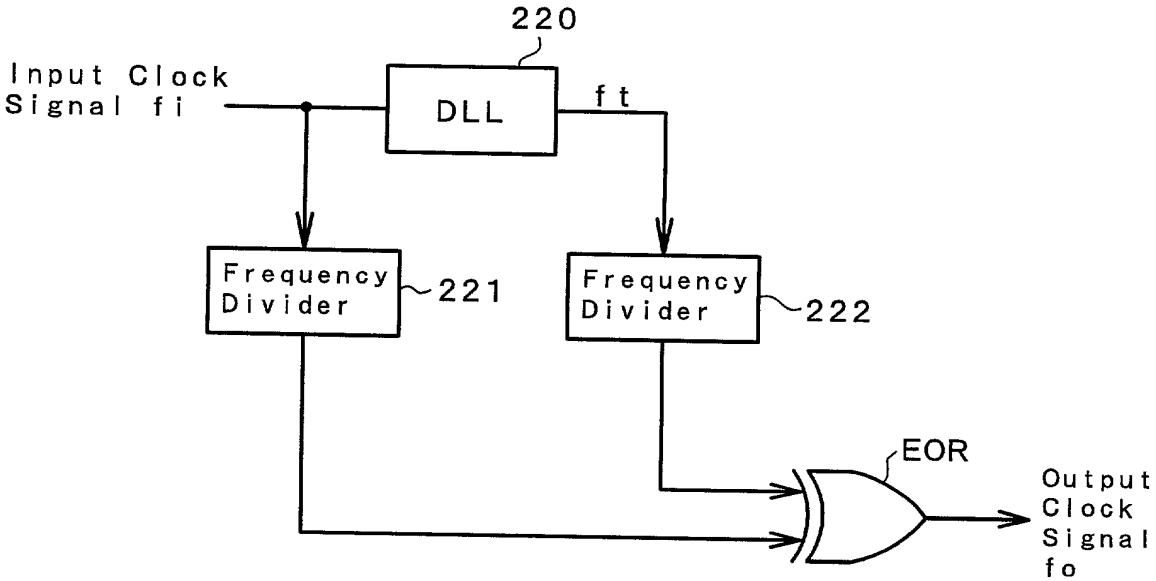

FIG. 6

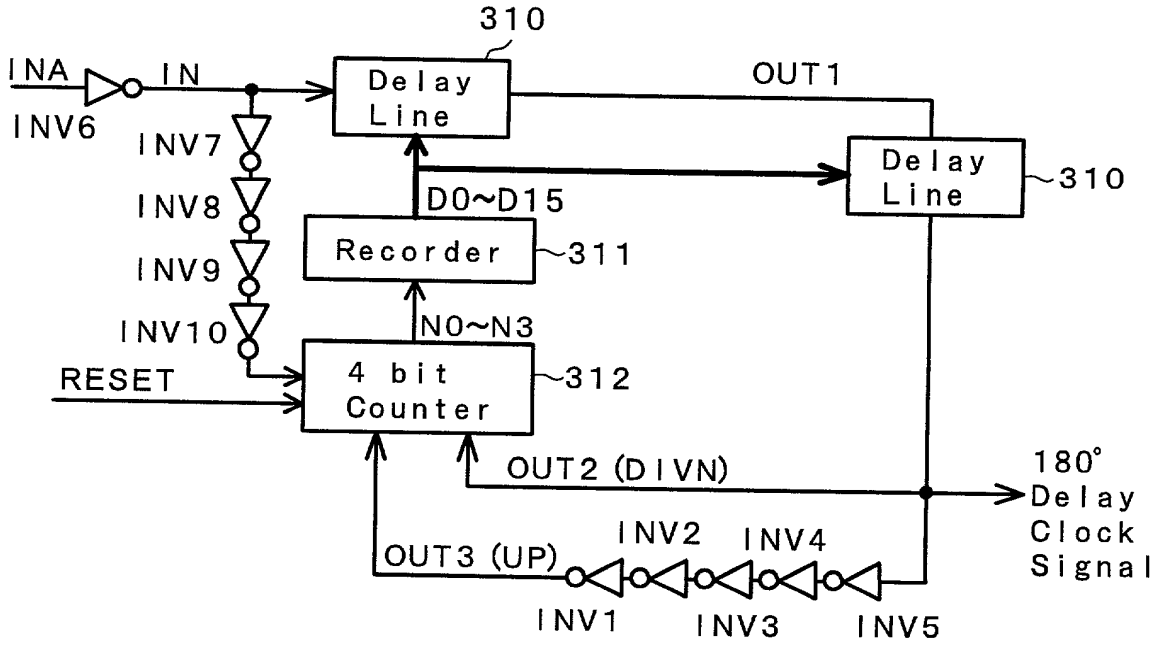
310
INA
IN
INV6
INV7
INV8
INV9
INV10
RESET
Delay Line
OUT1
Delay Line
310
D0~D15
Recorder
311
N0~N3
4 bit Counter
312
OUT2 (DIVN)
180° Delay Clock Signal
OUT3 (UP)
INV2
INV4
INV1
INV3
INV5

FIG. 7

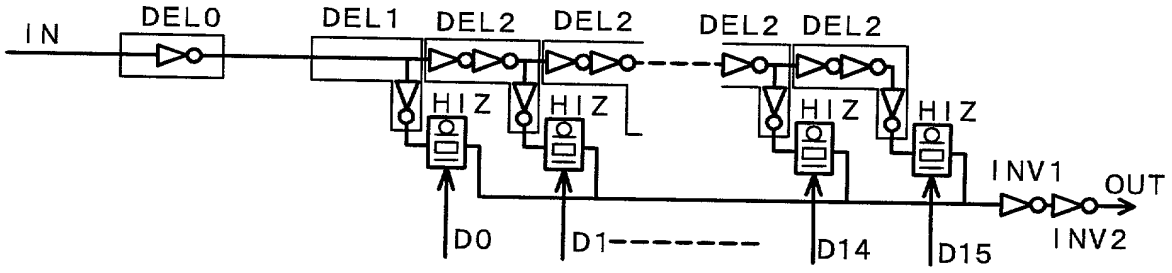
IN
DEL0
DEL1
DEL2
DEL2
DEL2
DEL2
HIZ
HIZ
HIZ
HIZ
INV1
OUT
INV2
D0
D1
D14
D15

FIG. 8

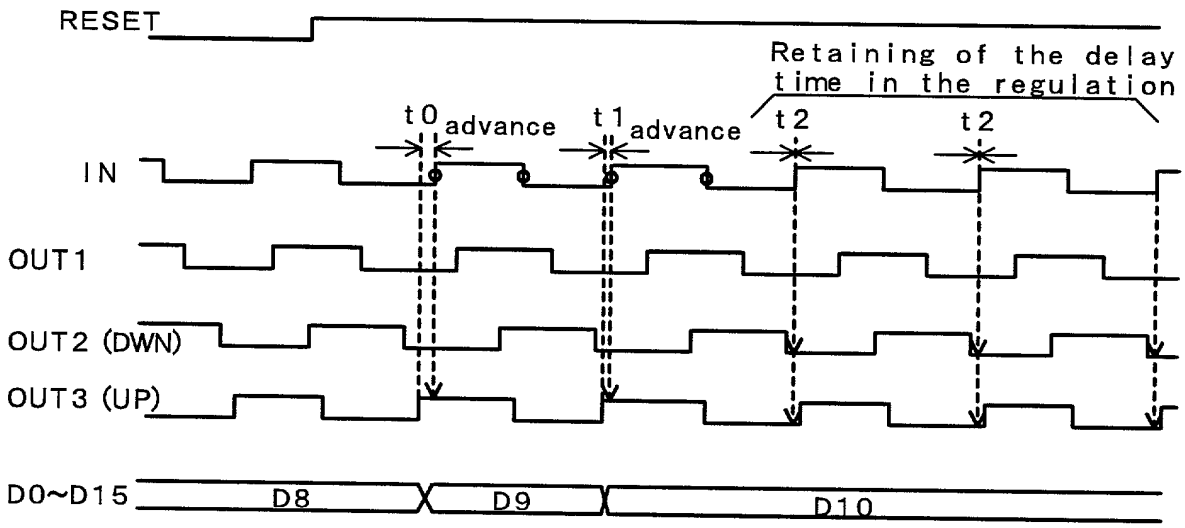
RESET
Retaining of the delay time in the regulation
t0 advance
t1 advance
t2
t2
IN
OUT1
OUT2 (DWN)
OUT3 (UP)
D0~D15
D8
D9
D10

FIG. 9

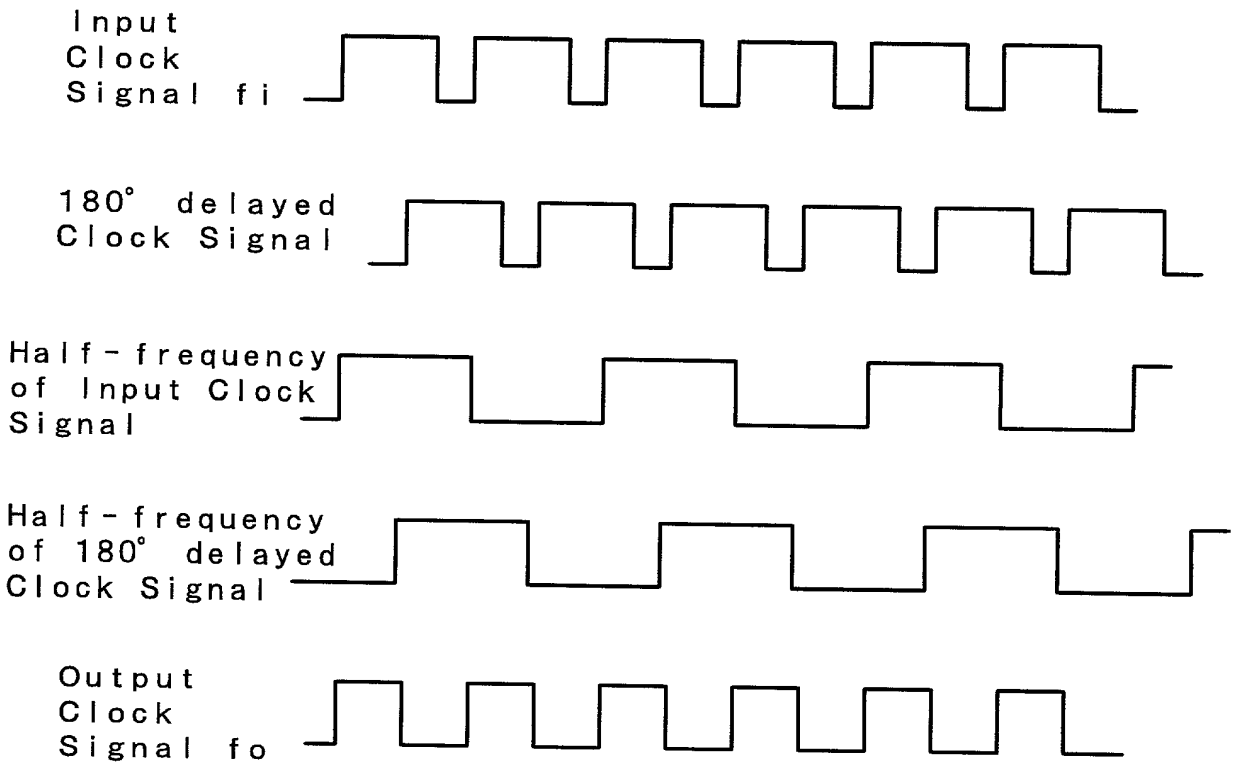
Input Clock Signal fi
180° delayed Clock Signal
Half-frequency of Input Clock Signal
Half-frequency of 180° delayed Clock Signal
Output Clock Signal fo

FIG. 10

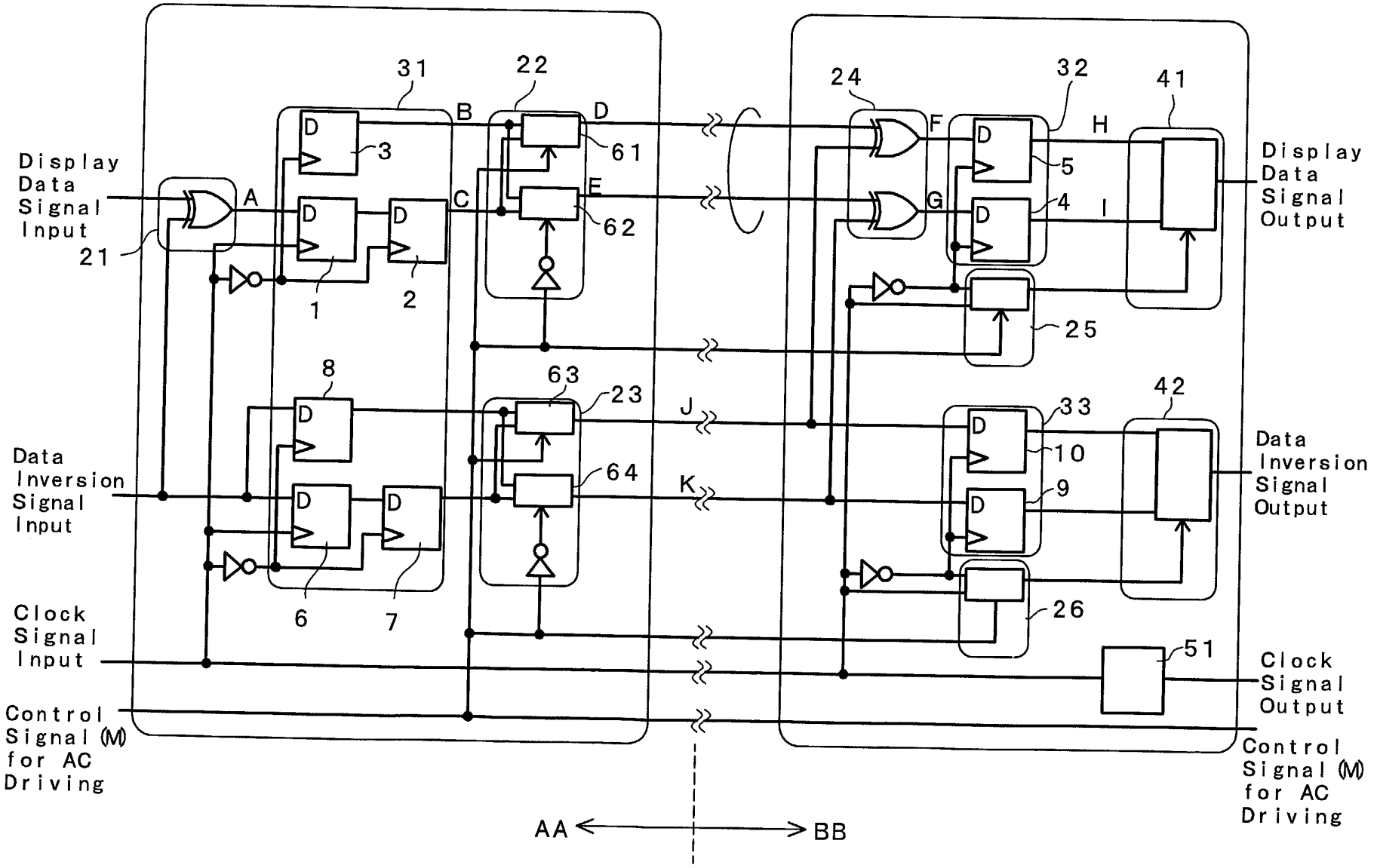
Display Data Signal Input
21
Data Inversion Signal Input
Clock Signal Input
Control Signal (M) for AC Driving
A
B
C
D
E
F
G
H
I
J
K
1
2
3
4
5
6
7
8
9
10
22
23
24
25
26
31
32
33
41
42
51
61
62
63
64
Display Data Signal Output
Data Inversion Signal Output
Clock Signal Output
Control Signal (M) for AC Driving
AA
BB

FIG. 11

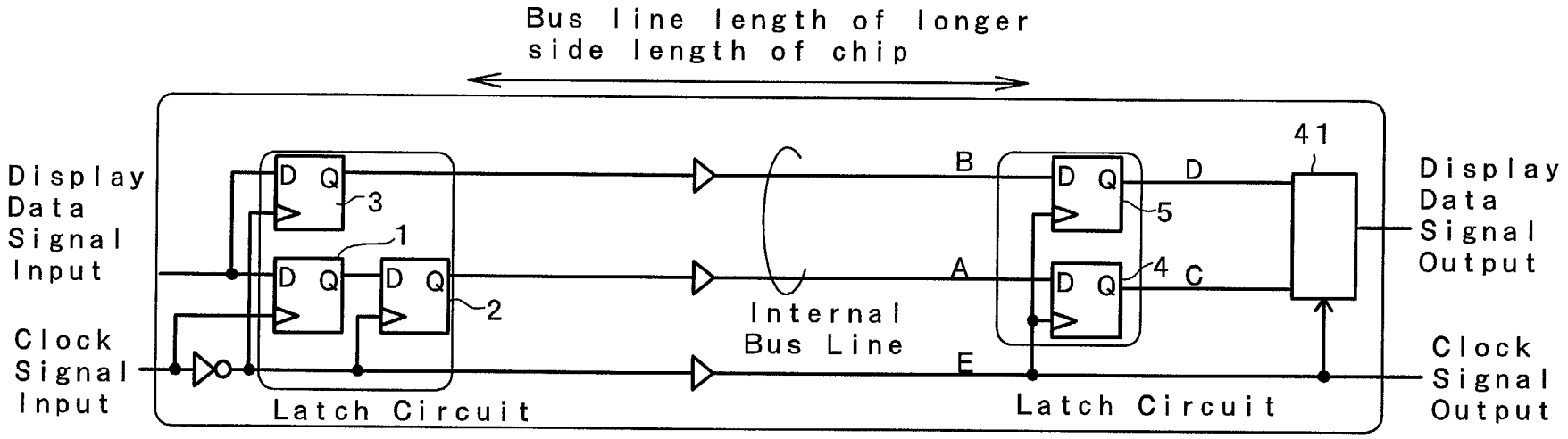
Bus line length of longer side length of chip
Display Data Signal Input
Clock Signal Input
D Q
3
1
2
Latch Circuit
Internal Bus Line
B
A
E
5
4
C
D
41
Latch Circuit
Display Data Signal Output
Clock Signal Output

FIG. 12

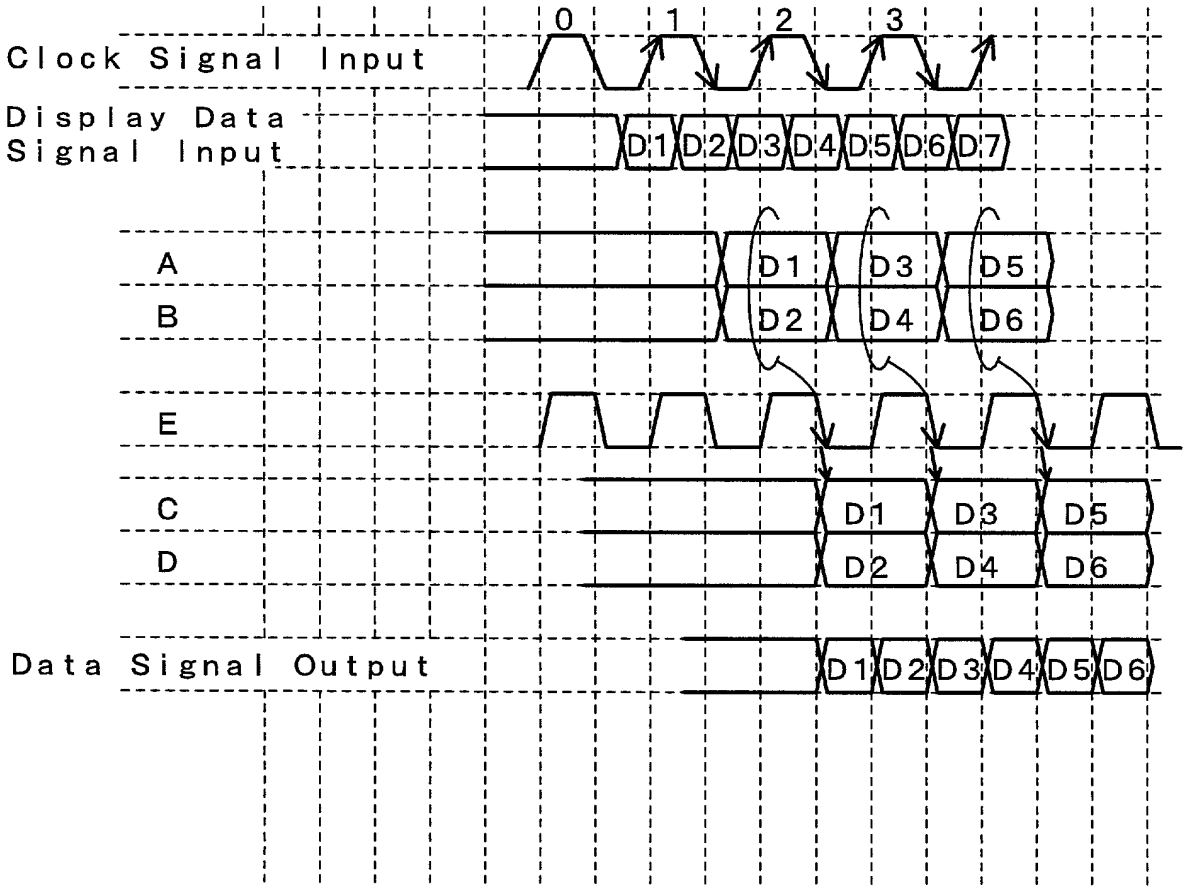
0
1
2
3
Clock Signal Input
Display Data Signal Input
D1 D2 D3 D4 D5 D6 D7
A
B
D1 D3 D5
D2 D4 D6
E
C
D
D1 D3 D5
D2 D4 D6
Data Signal Output
D1 D2 D3 D4 D5 D6

FIG. 13

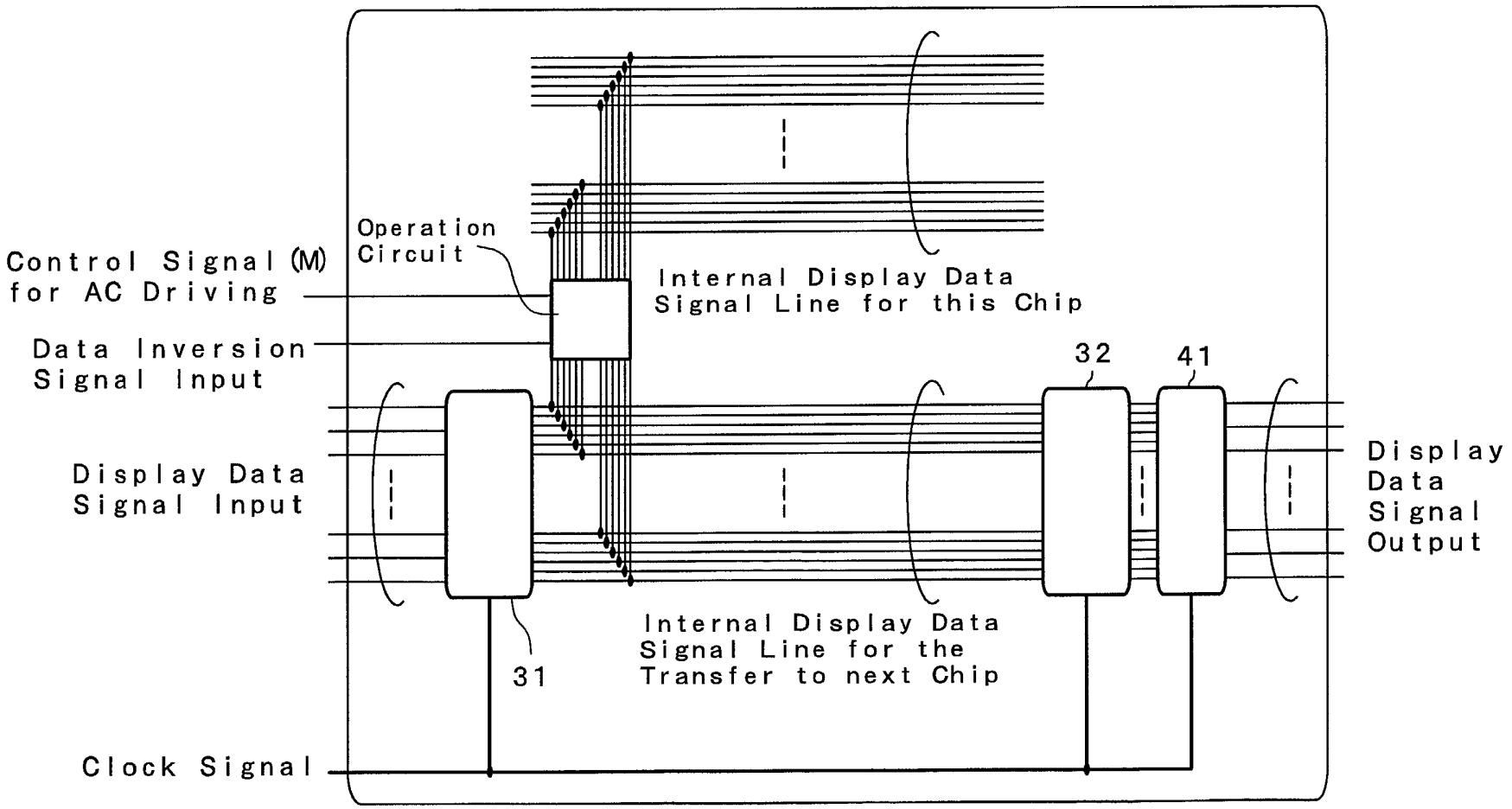
Operation Circuit
Control Signal (M) for AC Driving
Data Inversion Signal Input
Display Data Signal Input
Clock Signal
Internal Display Data Signal Line for this Chip
Internal Display Data Signal Line for the Transfer to next Chip
31
32
41
Display Data Signal Output

FIG. 14

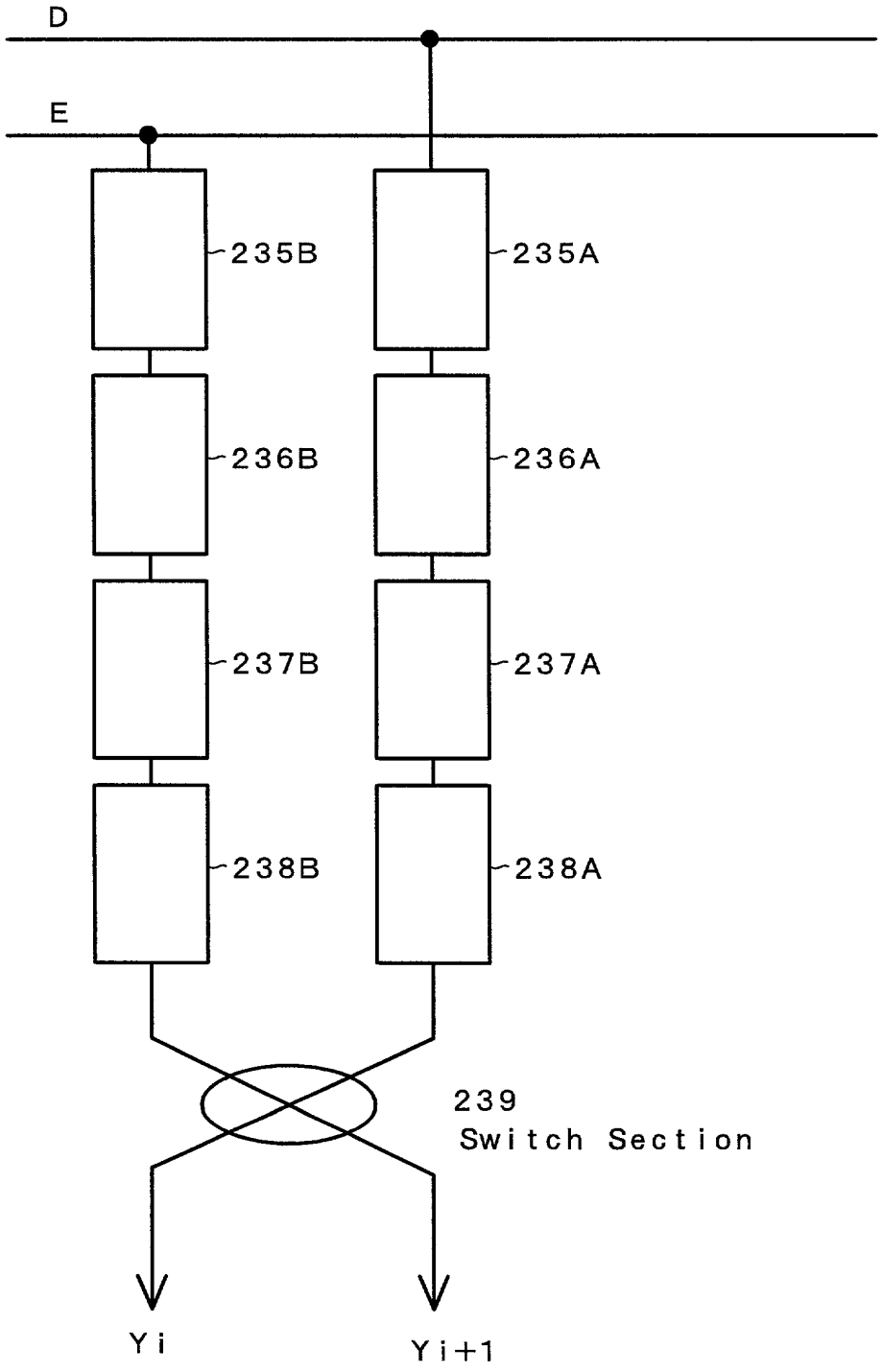
D
E
235B
235A
236B
236A
237B
237A
238B
238A
239
Switch Section
Yi
Yi+1

FIG. 15

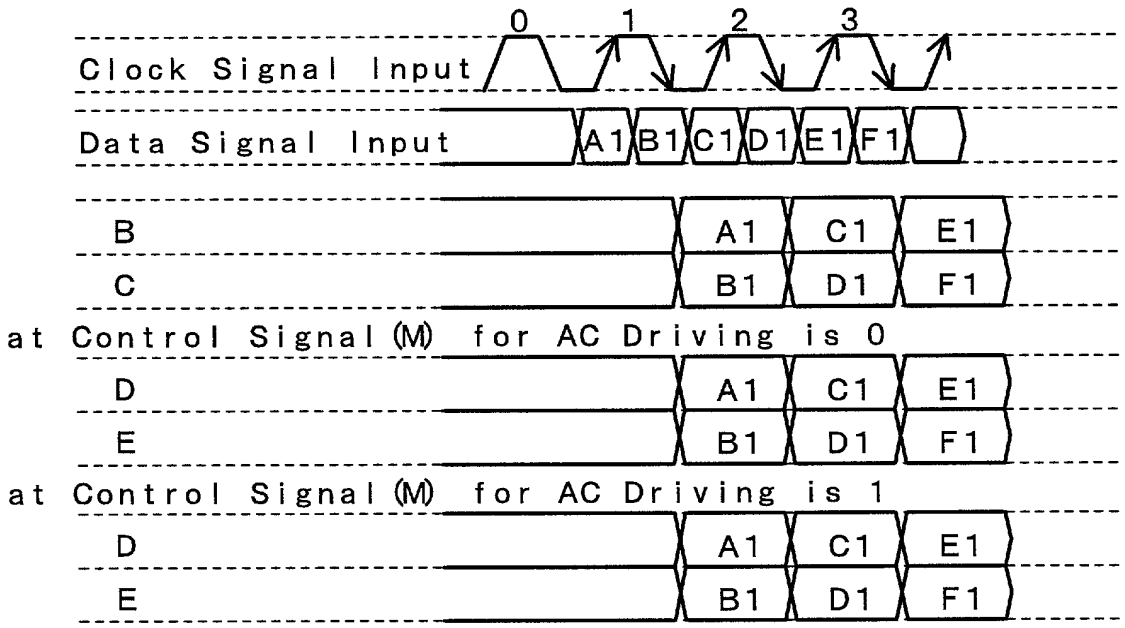

FIG. 16

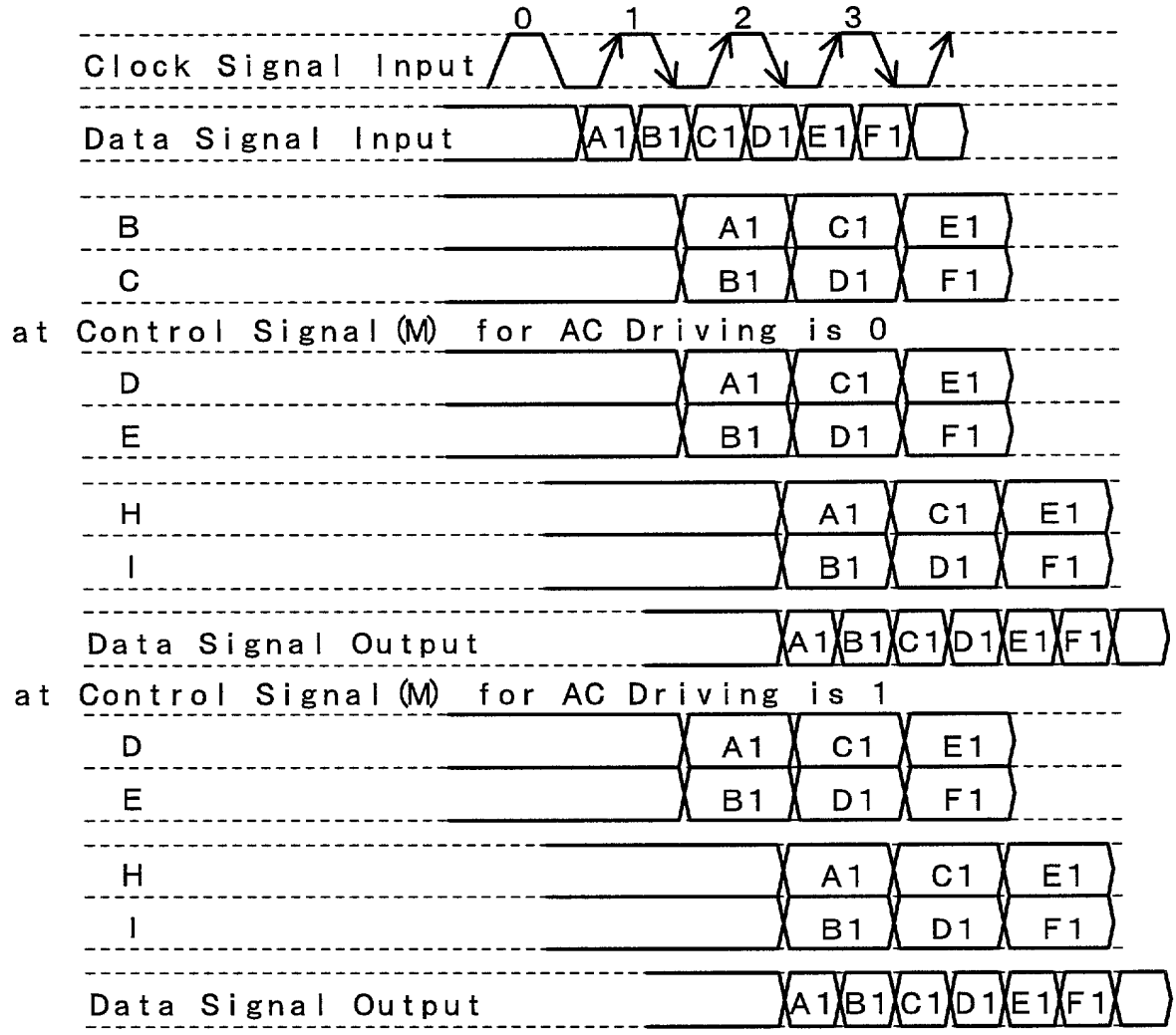

FIG. 17

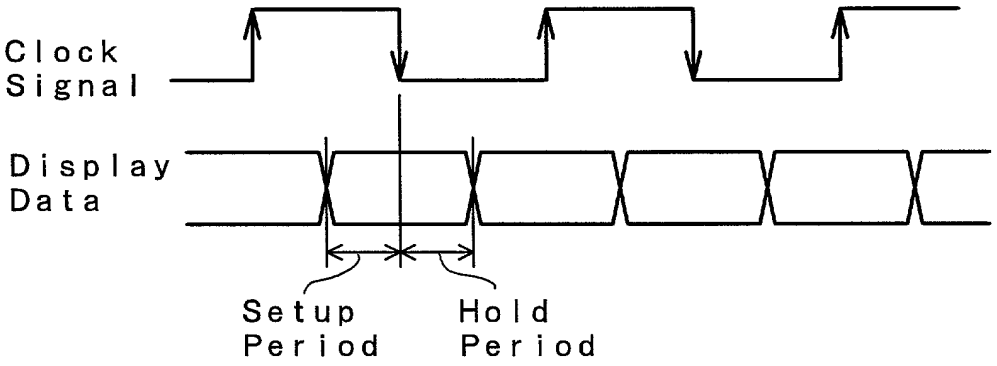

FIG. 18

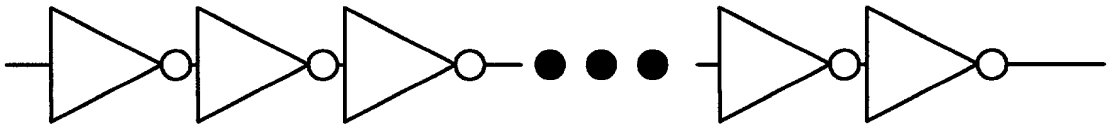

FIG. 19

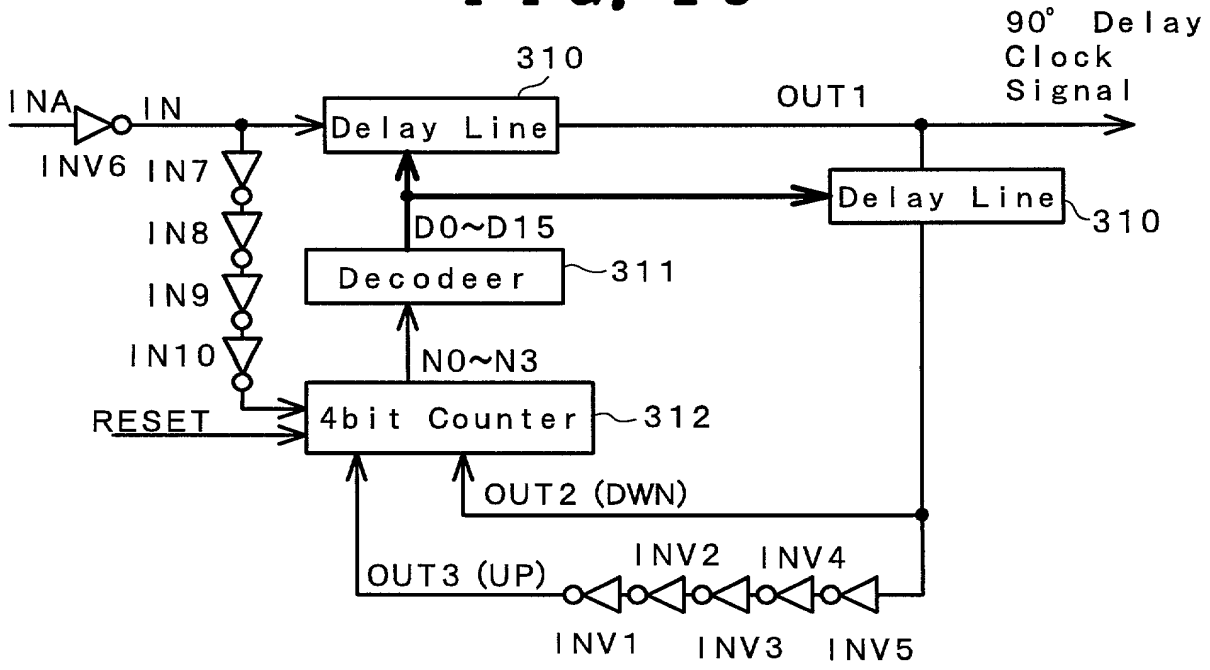

FIG. 20

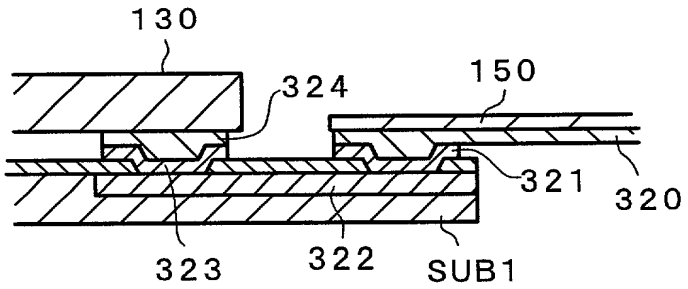
130
324
150
321
320
323
322
SUB1

FIG. 21

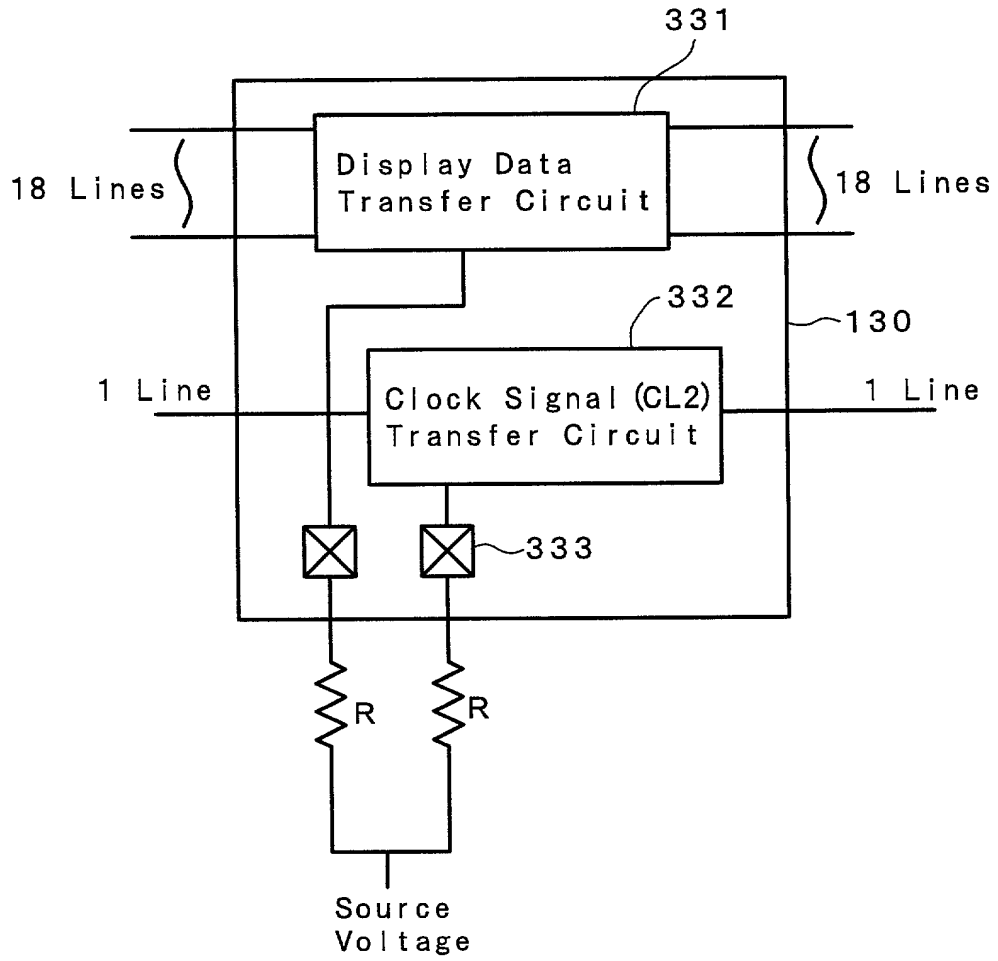
331
18 Lines
Display Data
Transfer Circuit
18 Lines
332
130
1 Line
Clock Signal (CL2)
Transfer Circuit
1 Line
333
R
R
Source
Voltage

FIG. 22

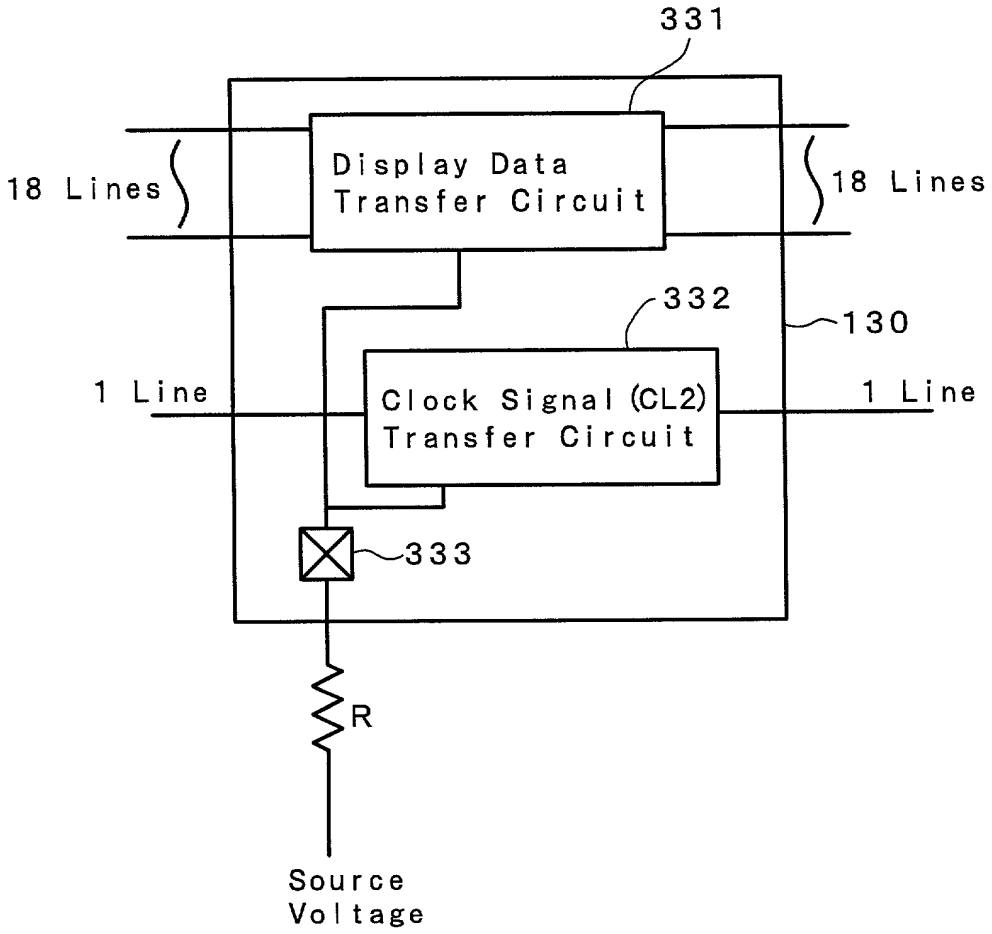
331
Display Data
Transfer Circuit
18 Lines
18 Lines
332
130
1 Line
Clock Signal (CL2)
Transfer Circuit
1 Line
333
R
Source
Voltage

FIG. 23

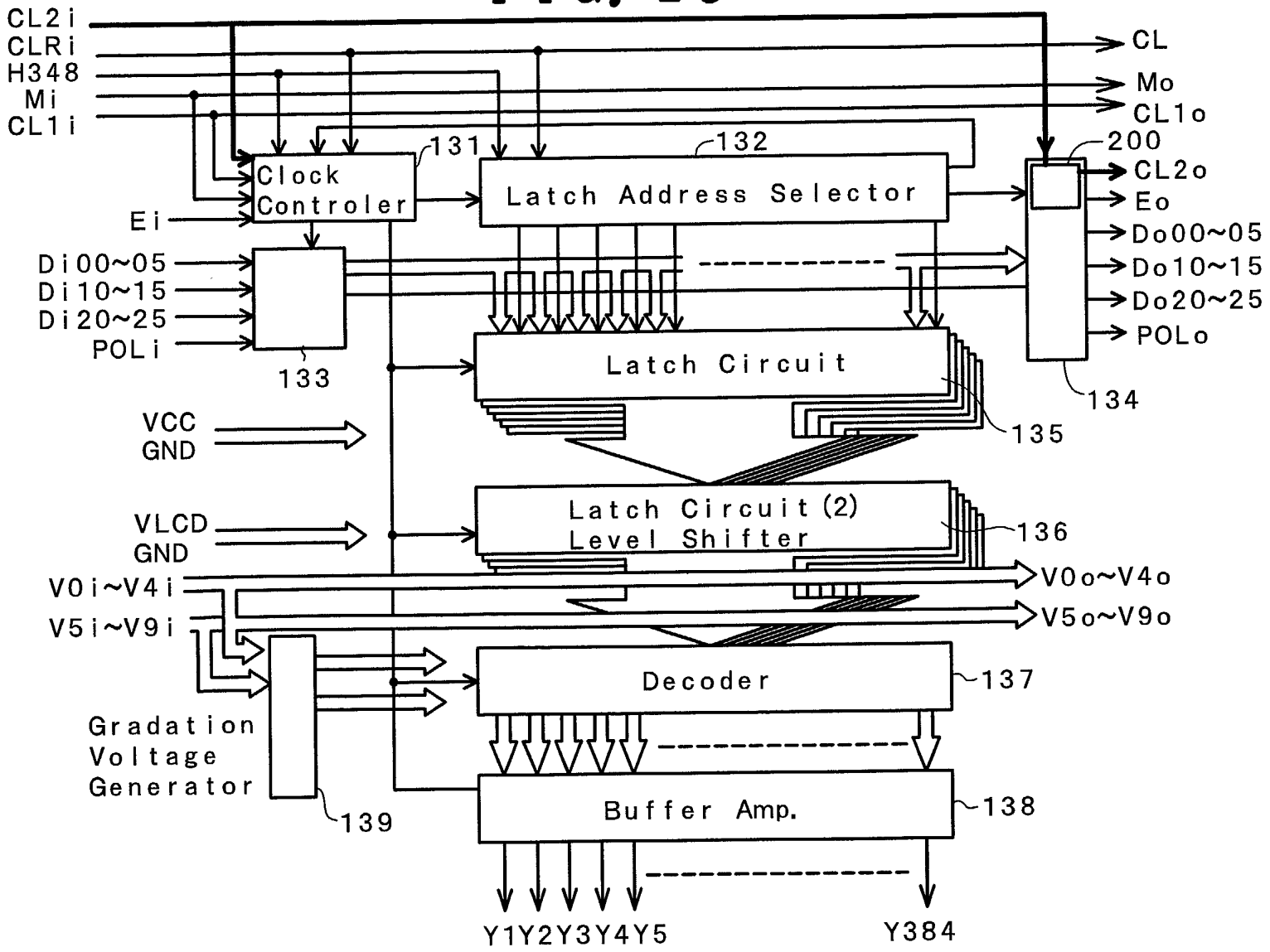
CL2i
CLRi
H348
Mi
CL1i
Clock Controler
131
132
Latch Address Selector
200
CL
Mo
CL1o
CL2o
Eo
Do00~05
Do10~15
Do20~25
POLo
Ei
Di00~05
Di10~15
Di20~25
POLi
133
Latch Circuit
134
135
VCC
GND
Latch Circuit (2)
Level Shifter
136
VLCD
GND
V0i~V4i
V5i~V9i
V0o~V4o
V5o~V9o
Decoder
137
Gradation
Voltage
Generator
139
Buffer Amp.
138
Y1Y2Y3Y4Y5
Y384

FIG. 24

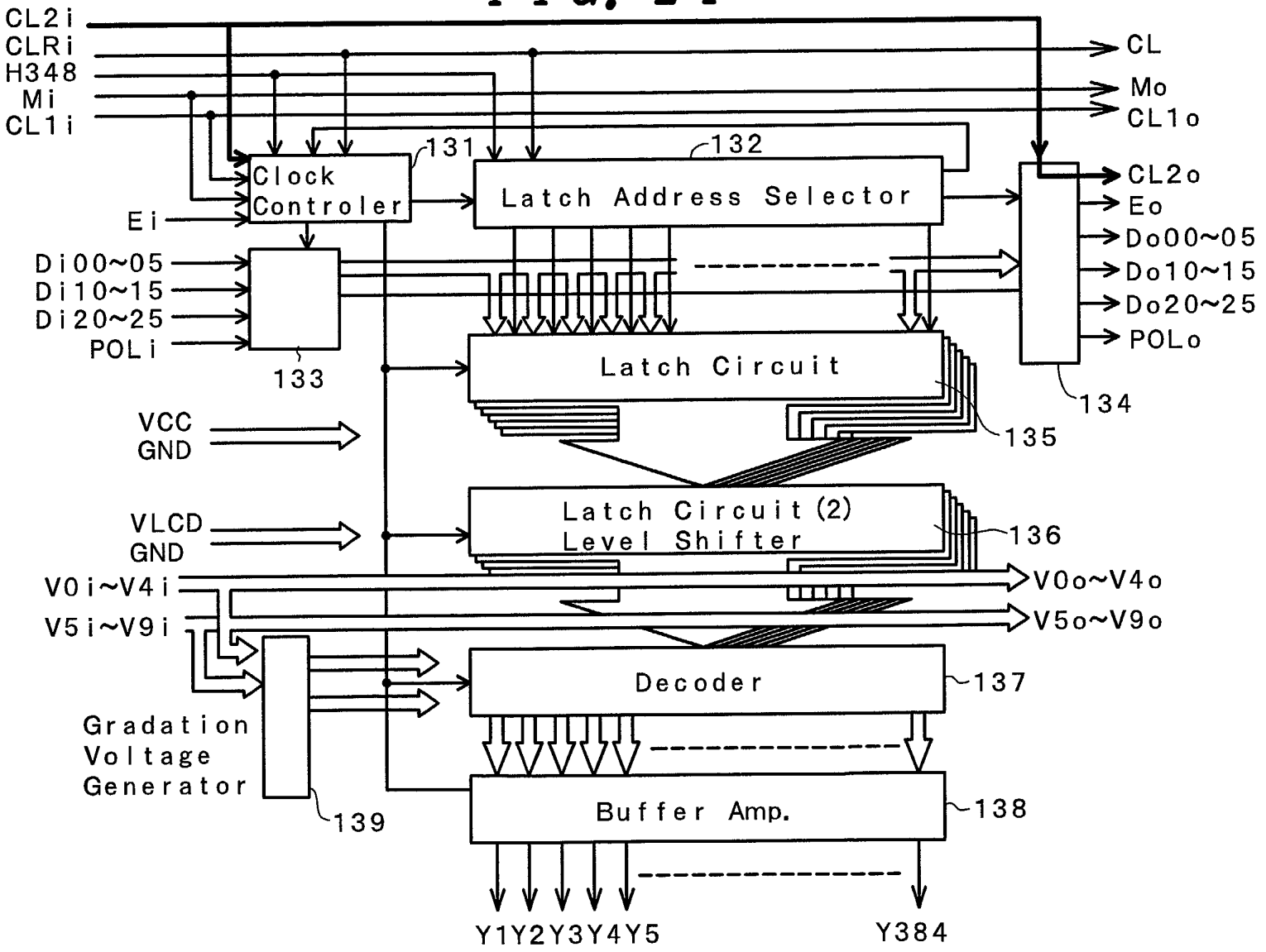
CL2i
CLRi
H348
Mi
CL1i
Ei
Di00~05
Di10~15
Di20~25
POLi
Clock Controler
131
132
Latch Address Selector
133
Latch Circuit
135
134
CL
Mo
CL1o
CL2o
Eo
Do00~05
Do10~15
Do20~25
POLo
VCC
GND
VLCD
GND
Latch Circuit (2) Level Shifter
136
V0i~V4i
V5i~V9i
V0o~V4o
V5o~V9o
Decoder
137
Gradation Voltage Generator
139
Buffer Amp.
138
Y1Y2Y3Y4Y5
Y384

FIG. 25

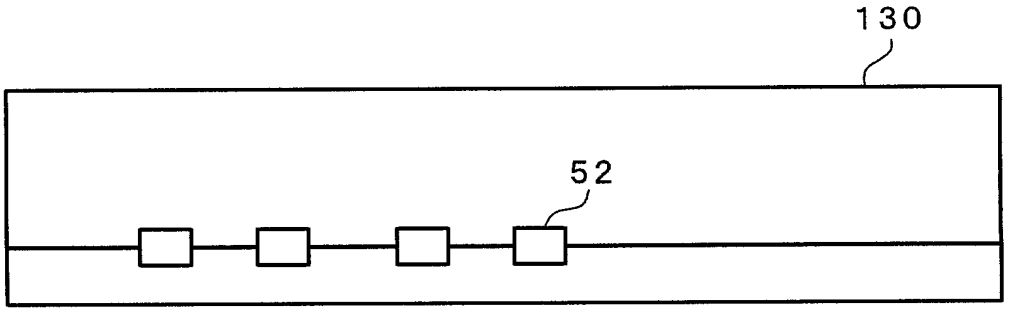
130
52

FIG. 26

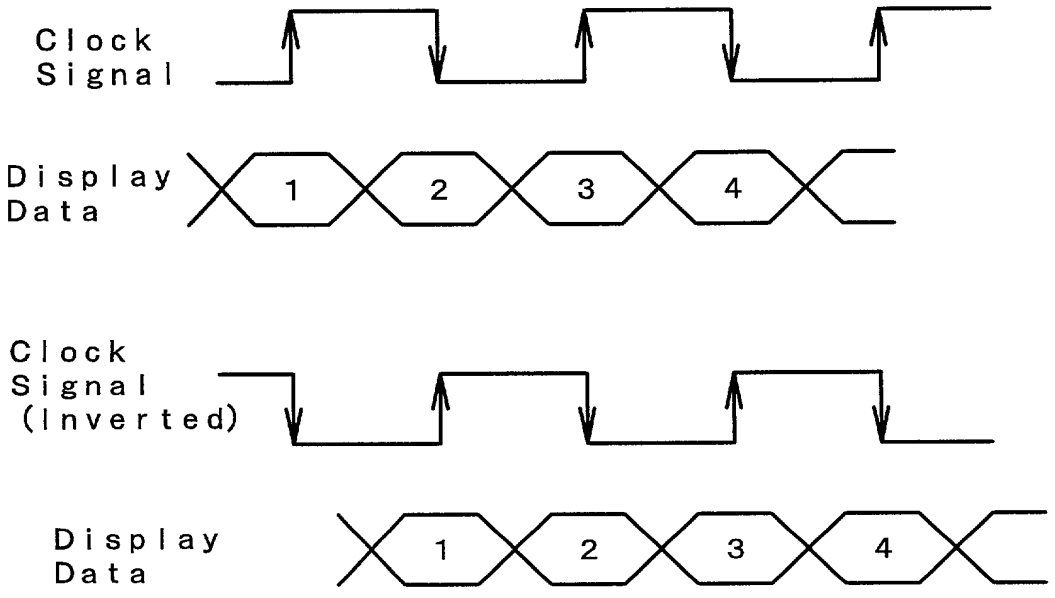
Clock Signal
Display Data
1
2
3
4
Clock Signal (Inverted)
Display Data
1
2
3
4

FIG. 27

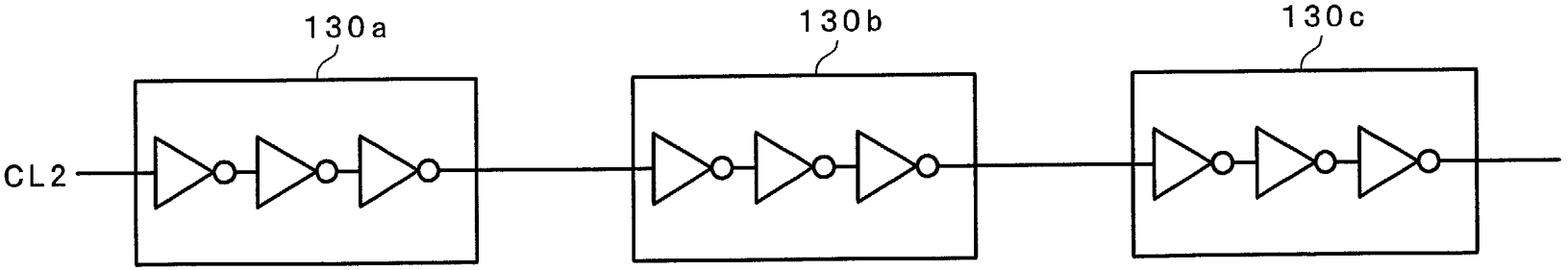

FIG. 28

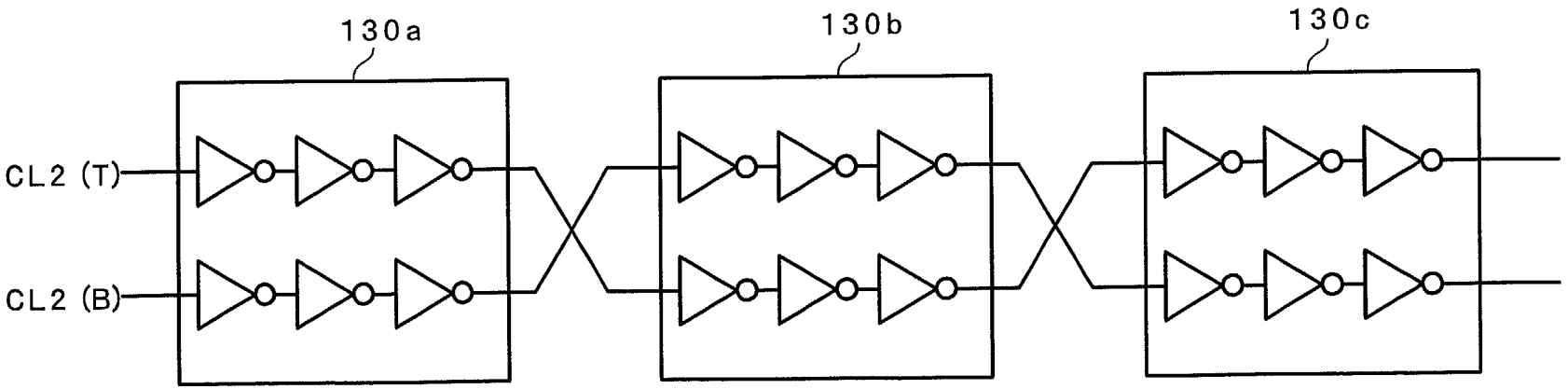

FIG. 29

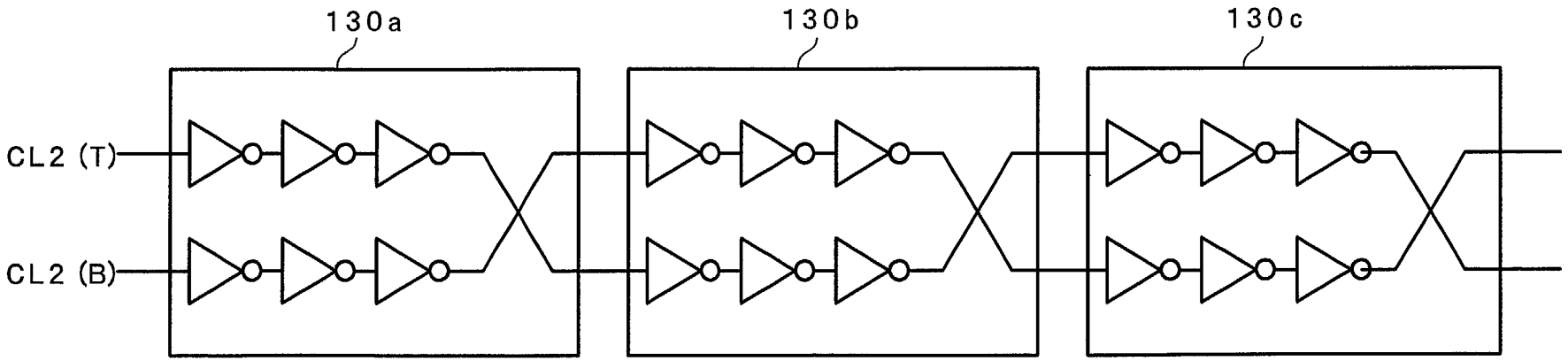

FIG. 30

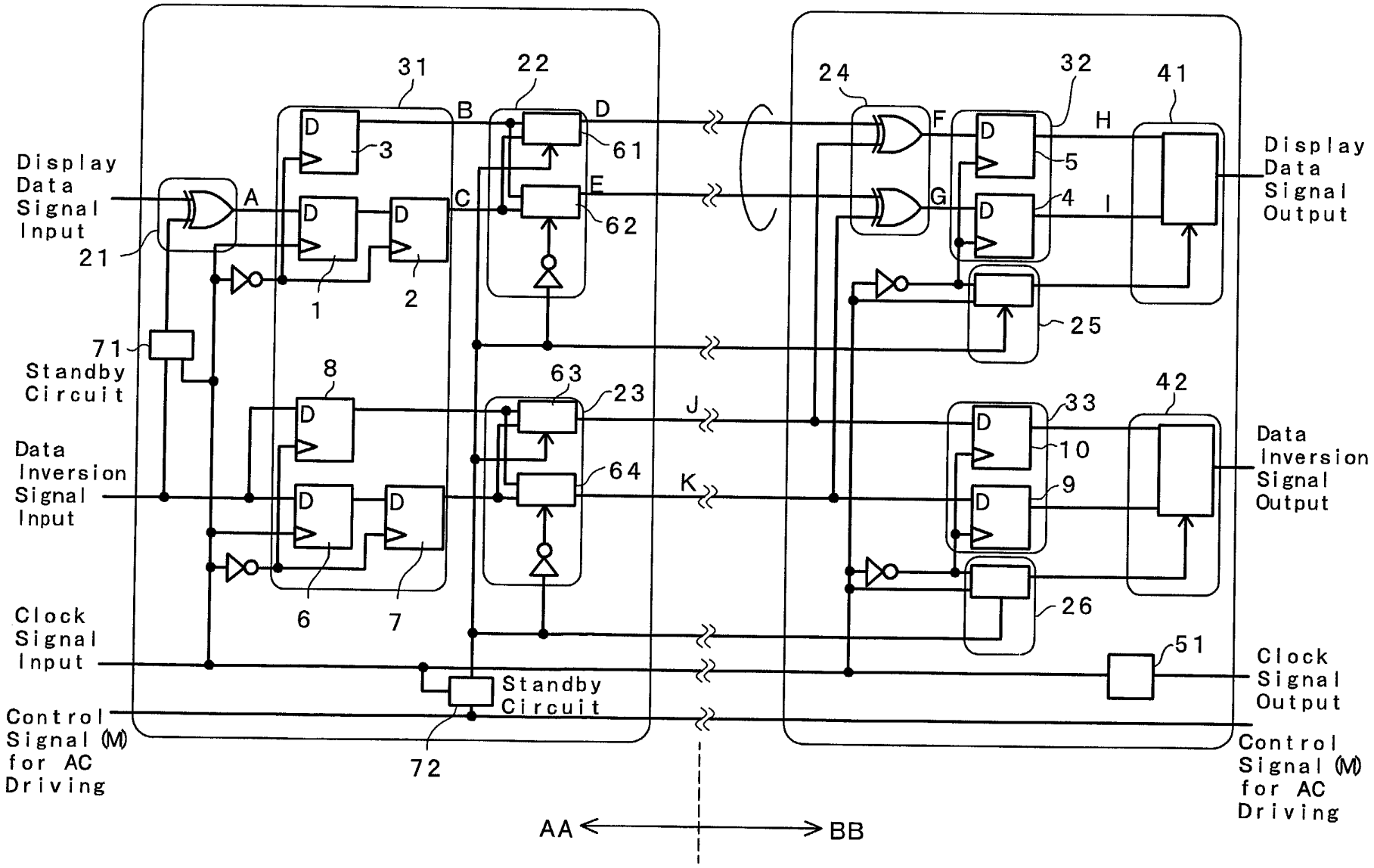
Display Data Signal Input
21
A
31
22
B
D
61
C
E
62
3
1
2
71
Standby Circuit
8
63
23
J
Data Inversion Signal Input
64
K
6
7
Clock Signal Input
Standby Circuit
Control Signal (M) for AC Driving
72
24
32
41
F
H
5
G
4
I
Display Data Signal Output
25
42
33
10
9
Data Inversion Signal Output
26
51
Clock Signal Output
Control Signal (M) for AC Driving
AA
BB

FIG. 31

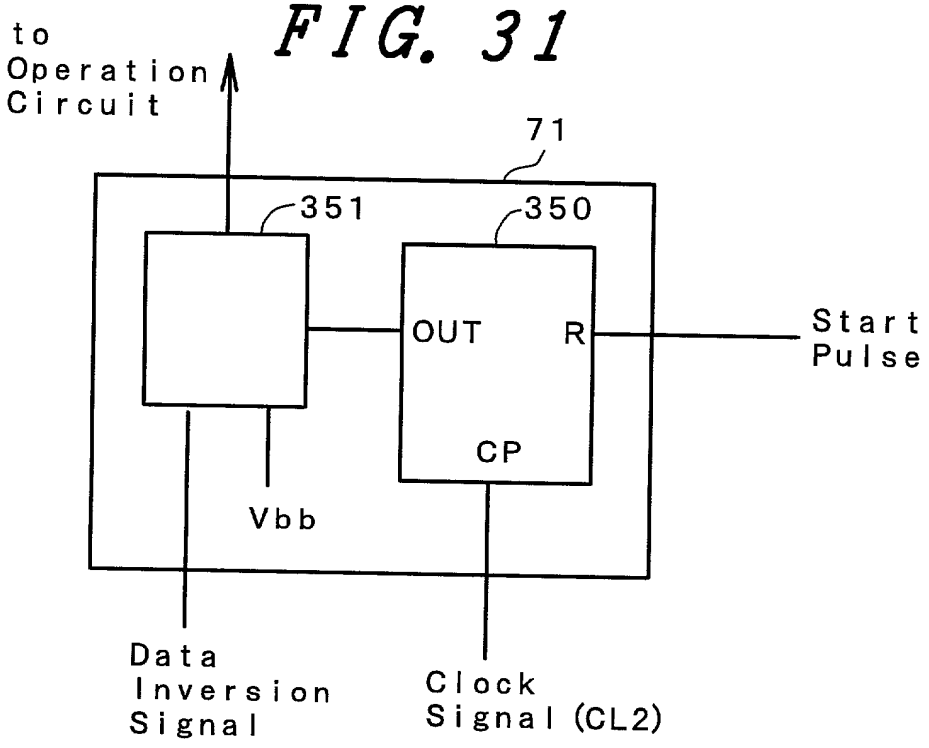

FIG. 32A Prior Art

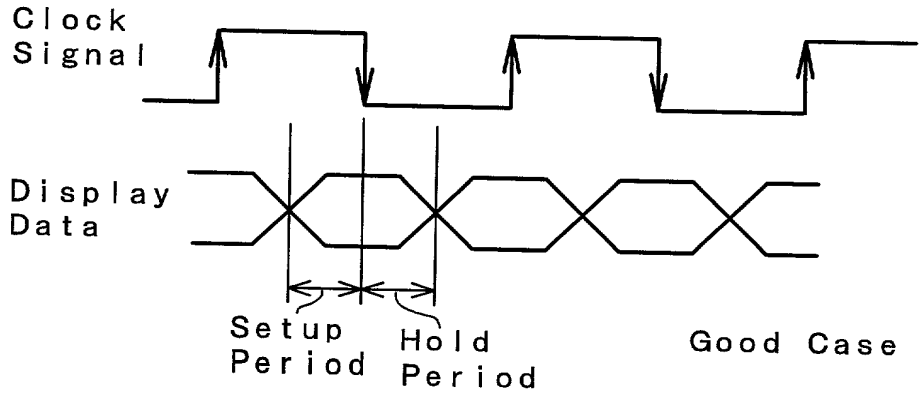

FIG. 32B Prior Art